In the claims:

1. (Original) A servo circuit, comprising:

a servo channel operable to recover servo data from servo wedges that identify respective data sectors on a data-storage disk; and

a processor coupled to the servo channel and operable to detect one of the servo wedges while the disk is attaining or after the disk attains an operating speed but before the servo channel recovers any servo data.

2. (Original) The servo circuit of claim 1 wherein the processor is operable to cause the servo channel to recover servo data from the one servo wedge after the processor detects the one servo wedge and before the servo channel recovers servo data from any other servo wedge.

3. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble; and

the processor is operable to detect the one servo wedge by detecting the preamble.

4. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble and a servo synchronization mark following the preamble;

the processor is operable to detect the one servo wedge by detecting the preamble; and

the servo channel is operable to recover the synchronization mark in response to the processor detecting the preamble.

5. (Original) The servo circuit of claim 1, wherein:

the one servo wedge and a servo wedge following the one servo wedge each comprise a preamble and a servo synchronization mark following the preamble;

the processor is operable to detect the one servo wedge by detecting the preamble of the one servo wedge;

the servo channel is operable to recover the synchronization mark of the one servo wedge in response to the processor detecting the preamble of the one servo wedge;

after detecting the one servo wedge, the processor is operable to detect the following servo wedge by detecting the preamble of the following servo wedge; and

the servo channel is operable to recover the synchronization mark of the following servo wedge in response to the processor detecting the preamble of the following servo wedge.

6. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the one servo wedge by,

summing even samples and summing odd samples to generate respective even and odd sums,

comparing the even sum and the odd sum with a threshold, and

detecting the one servo wedge if the even and odd sums are less than the threshold.

7. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the one servo wedge by,

averaging two of the even samples to generate an average even sample,

averaging two of the odd samples to generate an average odd sample,

summing the squares of the average even and odd samples,

comparing the sum of the squares to a threshold, and

detecting the one servo wedge if the sum of the squares is greater than the threshold.

8. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the one servo wedge by,

summing the respective squares of an even sample and an odd sample,

comparing the sum of the squares to a threshold, and

detecting the one servo wedge if the sum of the squares is greater than the threshold.

9. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the one servo wedge by,

summing the respective squares of an even sample and an odd sample,

calculating a square root of the sum of the squares,

comparing the square root to a threshold, and
detecting the one servo wedge if the square root is greater than the threshold.

10. (Original) The servo circuit of claim 1 wherein:
the one servo wedge comprises a preamble;
the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal;
the processor is operable to detect the one servo wedge by detecting the preamble from the samples;
the servo channel comprises an interpolator loop that acquires the timing of the samples with respect to the read signal while the processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble.

11. (Original) The servo circuit of claim 1 wherein:
the one servo wedge comprises a preamble;
the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal;
the processor is operable to detect the one servo wedge by detecting the preamble from the samples;
the servo channel comprises an interpolator loop that acquires the timing of the samples with respect to the read signal while the processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble; and
the processor is operable to stop the interpolator loop from tracking the timing of the samples if the processor fails to detect the preamble for at least a predetermined number of samples after the interpolator loop begins tracking the timing of the samples.

12. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal;

the processor is operable to detect the one servo wedge by detecting the preamble from the samples;

the servo channel comprises an interpolator loop that acquires the timing of the samples with respect to the read signal while the processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble; and

the processor is operable to stop the interpolator loop from tracking the timing of the samples if the processor fails to detect the preamble for at least eight samples after the interpolator loop begins tracking the timing of the samples.

13. (Original) The servo circuit of claim 1 wherein:

the one servo wedge comprises a preamble;

the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal; and

the processor is operable to detect the preamble if and only if a predetermined number of consecutive samples represent the preamble.

14. (Original) The servo circuit of claim 1, further comprising:

wherein the one servo wedge comprises a preamble;

wherein the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal;

wherein the processor is operable to detect the one servo wedge by detecting the preamble from the samples;

wherein the servo channel comprises an interpolator loop that acquires the timing of the samples with respect to the read signal while the

processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble; and

an initial-timing circuit operable to calculate an initial timing difference between the samples and the read signal and to provide an initial timing adjustment to the interpolator loop while the interpolator loop is acquiring the timing of the samples.

15. (Original) The servo circuit of claim 1, further comprising:

wherein the one servo wedge comprises a preamble;

wherein the servo channel is operable to generate a read signal that represents the servo wedge, to amplify the read signal with a gain, and to sample the read signal;

wherein the processor is operable to detect the one servo wedge by detecting the preamble from the samples; and

an initial-gain circuit operable to calculate an initial amplitude of the read signal and to provide an initial gain adjustment to the servo channel.

16. (Original) The servo circuit of claim 1 wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level.

17. (Original) The servo circuit of claim 1 wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than two consecutive logic 1's, the groups separated from each other by respective logic 0's.

18. (Original) The servo circuit of claim 1 wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than two consecutive logic 1's, the groups separated from each other by no more than ten and no fewer than two logic 0's.

19. (Original) The servo circuit of claim 1 wherein:

the servo wedge comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level; and

the servo channel comprises a Viterbi detector that excludes state transitions that are excluded from the predetermined binary sequence.

20. (Original) The servo circuit of claim 1 wherein:

the servo wedge comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level;

the servo channel is operable to generate a read signal that represents the servo wedge; and

the servo channel comprises a Viterbi detector that is operable to recover the binary sequence from the signal by,

calculating a respective path metric for each of no more than four possible states of the binary sequence, and

determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path.

21. (Original) The servo circuit of claim 1 wherein the one servo wedge lacks an erase field.

22. (Original) A servo circuit, comprising:

a servo channel operable to recover servo data that identifies a data sector before or during a read of or a write to the data sector, the servo data and the data sector located on a data-storage disk; and

a processor coupled to the servo channel and operable to detect the servo data after the disk has attained an operating speed but before the

servo channel has recovered any servo data from the data-storage disk.

23. (Original) The servo circuit of claim 22 wherein the servo channel is operable to recover the servo data after the processor has detected the servo data but before the servo channel has recovered any other servo data from the data-storage disk.

24. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble; and

the processor is operable to detect the servo data by detecting the preamble.

25. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble and a servo synchronization mark following the preamble;

the processor is operable to detect the servo data by detecting the preamble; and

the servo channel is operable to recover the synchronization mark in response to the processor detecting the preamble.

26. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the servo data by,

summing even samples and summing odd samples to generate respective even and odd sums,

comparing the even sum and the odd sum with a threshold, and

detecting the servo data if the even and odd sums are less than the threshold.

27. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the servo data by,

averaging two of the even samples to generate an average even sample,

averaging two of the odd samples to generate an average odd sample,

summing the squares of the average even and odd samples,

comparing the sum of the squares to a threshold, and

detecting the servo data if the sum of the squares is greater than the threshold.

28. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a sinusoidal read signal that represents the preamble and to sample the read signal at approximately 90° intervals with respect to the read signal; and

the processor is operable to detect the servo data by,

summing the respective squares of an even sample and an odd sample,

calculating a square root of the sum of the squares,

comparing the square root to a threshold, and

detecting the servo data if the square root is greater than the threshold.

29. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a read signal that represents the servo data and to sample the read signal;

the processor is operable to detect the servo data by detecting the preamble from the samples;

the servo channel comprises an interpolator loop that coarsely adjusts respective phase angles of the samples with respect to the read signal while the processor is detecting the preamble and that finely adjusts the phase angles of the samples a predetermined time after the processor detects the preamble.

30. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a read signal that represents the servo data and to sample the read signal;

the processor is operable to detect the one data wedge by detecting the preamble from the samples;

the servo channel comprises an interpolator loop that coarsely adjusts respective phase angles of the samples with respect to the read signal while the processor is detecting the preamble and that finely adjusts the phase angles of the samples a predetermined time after the processor detects the preamble; and

the processor is operable to stop the interpolator loop from finely adjusting the phase angles of the samples if the processor fails to detect the preamble for at least a predetermined number of samples after the interpolator loop begins finely adjusting the phase angles of the samples.

31. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a preamble;

the servo channel is operable to generate a read signal that represents the servo data and to sample the read signal; and

the processor is operable to detect the preamble if and only if a predetermined number of consecutive samples represent the preamble.

32. (Original) The servo circuit of claim 22, further comprising:

wherein the servo data comprises a preamble;

wherein the servo channel is operable to generate a read signal that represents the servo data and to sample the read signal;

wherein the processor is operable to detect the servo data by detecting the preamble from the samples;

wherein the servo channel comprises an interpolator loop that coarsely adjusts respective phase angles the samples with respect to the read signal while the processor is detecting the preamble and that finely adjusts the phase angles of the samples a predetermined time after the processor detects the preamble; and

an initial-phase circuit operable to calculate an initial phase angle between a sample and the read signal and to provide an initial phase-angle adjustment to the interpolator loop while the interpolator loop is coarsely adjusting the phase angles of the samples.

33. (Original) The servo circuit of claim 22, further comprising:

wherein the servo data comprises a preamble;

wherein the servo channel is operable to generate a read signal that represents the servo data, to amplify the read signal with a gain, and to sample the read signal;

wherein the processor is operable to detect the one servo data by detecting the preamble from the samples; and

an initial-gain circuit operable to calculate an initial amplitude of the read signal and to provide an initial gain adjustment to the servo channel.

34. (Original) The servo circuit of claim 22 wherein the servo data comprises a binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level.

35. (Original) The servo circuit of claim 22 wherein the servo data comprises a binary sequence having groups of no more and no fewer than two consecutive logic 1's, the groups separated from each other by respective logic 0's.

36. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level; and

the servo channel comprises a Viterbi detector that excludes state transitions that are excluded from the predetermined binary sequence.

37. (Original) The servo circuit of claim 22 wherein:

the servo data comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level;

the servo channel is operable to generate a read signal that represents the servo data; and

the servo channel comprises a Viterbi detector that is operable to recover the binary sequence from the signal by,

calculating a respective path metric for each of no more than four possible states of the binary sequence, and

determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path.

38. (Original) A method, comprising:

rotating a data-storage disk having a surface from a first rotational speed to a second rotational speed over a first time period, the cirumferential position of a read head relative to a location of the disk surface being unknown for a portion of the first time period;

during or after the first time period and while the circumferential position of the read head is unknown, detecting servo data that identifies application data stored on the data-storage disk; and

determining the circumferential position of the read head from the detected servo data.

39. (Original) The method of claim 38 wherein the first rotational speed is zero or is approximately zero.

40. (Original) The method of claim 38 wherein the second rotational speed is a steady-state speed or is approximately a steady-state speed.

41. (Original) The method of claim 38 wherein the circumferential position of the read head is unknown for the entire first time period.

42. (Original) The method of claim 38 wherein the circumferential position of the read head is unknown for the entire first time period and for a second time period that follows and that is contiguous with the first time period.

43. (Original) The method of claim 38 wherein detecting the servo data comprises detecting a preamble that composes the servo data.

44. (Original) The method of claim 38 wherein determining the circumferential position of the read head comprises:

recovering a data-location identifier from the servo data; and

determining the circumferential position of the read head from the data-location identifier.

45. (Original) The method of claim 38 wherein detecting the servo data comprises accurately detecting a predetermined number of servo wedges before determining the circumferential position of the read head.

46. (Original) The method of claim 38 wherein detecting the servo data comprises accurately detecting three servo wedges before determining the circumferential position of the read head.

47. (Original) The method of claim 38 wherein detecting the servo data comprises:
summing even samples and summing odd samples of the servo data to generate respective even and odd sums;
comparing the even sum and the odd sum with a threshold; and
detecting the servo data if the even and odd sums are less than the threshold.

48. (Original) The method of claim 38 wherein detecting the servo data comprises:
averaging two even samples of the servo data to generate an average even sample;
averaging two odd samples of the servo data to generate an average odd sample;
summing the squares of the average even and odd samples;
comparing the sum of the squares to a threshold; and
detecting the servo data if the sum of the squares is greater than the threshold.

49. (Original) The method of claim 38 wherein detecting the servo data comprises:
summing respective squares of an even sample and an odd sample of the servo data;
comparing the sum of the squares to a threshold; and
detecting the servo data if the sum of the squares is greater than the threshold.

50. (Original) The method of claim 38 wherein detecting the servo data comprises:
summing respective squares of an even sample and an odd sample of the servo data;
calculating a square root of the sum of the squares;
comparing the square root to a threshold; and
detecting the servo data if the square root is greater than the threshold.

51. (Original) The method of claim 38 wherein detecting the servo data comprises:
sampling the servo data; and

synchronizing the samples to the servo data by interpolating values of synchronized samples of the servo data from actual values of respective unsynchronized samples of the servo data.

52. (Original) The method of claim 38 wherein detecting the servo data comprises:
sampling the servo data;
synchronizing the samples to the servo data by interpolating values of synchronized samples of the servo data from actual values of respective unsynchronized samples of the servo data; and
stop synchronizing the samples to the servo data if a preamble is not detected within a predetermined number of synchronized samples.

53. (Original) The method of claim 38 wherein detecting the servo data comprises detecting the servo data if and only if a predetermined number of consecutive samples of the servo data represent a preamble.

54. (Original) The method of claim 38 wherein detecting the servo data comprises:
sampling the servo data;
determining an initial difference between an actual sampling time and a desired sampling time;
synchronizing a sample to the desired sampling time by interpolating the sample based on the initial difference.

55. (Original) The method of claim 38 wherein detecting the servo data comprises:
amplifying the servo data by an amplification factor;
determining an initial amplitude of the amplified servo data; and
adjusting the amplification factor based on the initial amplitude.

56. (Original) The method of claim 38 wherein the servo data comprises a binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic

level, the groups separated from each other by respective bits having a second logic level.

57. (Original) The method of claim 38 wherein:

the servo data comprises a predetermined binary sequence; and

determining the position of the read head comprises recovering the detected servo data by excluding state transitions that are excluded from the predetermined binary sequence.